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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,311	10/07/2003	Francis Lin	P/727-116	5456
2352	7590	05/26/2006	EXAMINER	
OSTROLENK FABER GERB & SOFFEN 1180 AVENUE OF THE AMERICAS NEW YORK, NY 100368403			BEHSHAD, SHAHRAM	
			ART UNIT	PAPER NUMBER
			1756	

DATE MAILED: 05/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/680,311

Applicant(s)

LIN ET AL.

Examiner

Shah Behshad

Art Unit

1756

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 October 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 07 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application (PTO-152) |
| 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 3 states "wherein the integrated circuit forming steps include at least one of photoresist developing, photoresist baking, photoresist removing or etching, and depositing and or doping". The recitation "depositing and or doping" is not clear as to its meaning. Claims 4 and 5 are also rejected because they are dependent on claim 3.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-6 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by Pierrat et. al. (Patent No. 6646722)

Pierrat et. al. disclose an invention where a multiple-image reticle is used to form integrated circuitry comprising a two dimensional array of spaced images arranged in a matrix of controllably spaced rows and columns of images on a single reticle. By controlling which image is used and accurately positioning the wafer via the stepper, multiple images are accurately registered. Figure 1 is an image of the mask used in the invention by Pierrat et. al. With reference to figure 1, a multi image reticle 10 comprises a transparent substrate which is generally planar and essentially free of defects. After the reticle 10 has been polished, cleaned and inspected, it is ready to be coated by reflective material to form multiple integrated circuit mask patterns or images 112a, 112b, 112c, 112d, 112e, 112f, 112g, 112h, and 112 I which are spaced in rows and columns in a rectangular array (column 4, lines 5-10). These are 9 such images shown in Figure 1. In a refractive or transmissive photo mask as described with reference to Figure 2, radiation is transmitted through the reticle to expose a photo resist in a desired pattern on a semiconductor wafer (column 4, lines 26-29).

Each of the images in a reticle 211 comprises suitable patterns for forming circuitry on a suitable prepared substrate of a semiconductor wafer as shown at 210 in Figure 2 (column 4, lines 44-46). Since many identical circuits are formed on wafer 210, stepper 230 is used to step the radiation pattern through each of the separate circuits, referred to as a die (column 5,

lines 4-6). Images may be of different sizes and shapes as shown in the reticle 211 of Figure 2. (column 5, lines 38-39). The mask used by Pierrat et. al. clearly reads on the mask disclosed by the instant invention because the mask taught by Pierrat et. al. has more than one pattern on it and the patterns are not identical.

Each of the images in a reticle 211 comprise suitable patterns for forming circuitry on a suitably prepared substrate of a semiconductor wafer as shown at 210 in Fig. 2.

Pierrat et. al. claim a method of forming a die for a single integrated circuit on substrate, comprising:

Fabricating a reticle, positioning a plurality of integrated-circuit mask patterns in different areas of the reticle. Projecting radiation onto a first of the mask patterns to expose the die with a first of mask patterns on the reticle, processing the substrate in response to the first of the mask patterns, moving at least one of the die and the reticle relative to each other in a straight line without rotation; projecting radiation onto a second of the mask patterns to expose the same die with a second of the mask patterns on the reticle and fabricating at least one circuit layer on the substrate. (claim 6)

Based on claim 6, Pierrat et. al. disclose a processing step in between the two exposure steps. The processing step disclosed by Pierrat et. al. clearly reads on part of claim 1 of the instant invention where the wafer is subjected to subsequent integrated forming steps.

The steps outlined by the reference by Pierrat et. al. used to form integrated circuitry read on the claims of the instant invention. The steps are carried out in the same exact order of the instant invention.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-6 are rejected under 35 U.S.C. 102(a) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Hsu et. al. Hsu et. al. (Patent No. 6696227) disclose an invention where a multi-exposure method for defining a regular pattern by a photomask is presented. The method comprises forming a first region and a second region on a substrate. A first pattern is defined on the first region by a photomask. Next, the photomask is moved a predetermined distance and a second pattern is defined on the second region by the photomask. Finally, development is performed to display the first pattern and the second pattern on the photoresist layer. (see abstract)

Figure 2 depicts the pattern to be printed in the invention by Hsu et. al.

There are two groups of patterns in Figure 2. The first group of patterns

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comprises pattern elements 211-213, and the second group of patterns comprises pattern elements 221-223. (column 2, lines 29-34) The mask disclosed by Hsu et. al. reads on the mask disclosed by the instant invention because it has two patterns. A substrate 31 is provided. The surface or inside of the substrate 31 may comprise some structures, such as wells or oxide layers. Next, a photoresist 32, comprising a first region and a second region is formed on the substrate 31. Here, the first region corresponds to the region comprising patterns 411-413 in figure 4A, and a second region corresponds to the region comprising patterns 421-423 in figure 4B. Next, patterns 411-413 are defined on the first region of photoresist 31 by photomask 40. (column 2, lines 55-56) Next, the photomask 40 is shifted with a predetermined distance D, then patterns 421-423 are defined on the second region of the photomasks 40. This step reads on the step of claim 1 of the instant invention where the second image corresponding to the second mask pattern is formed. Finally, patterns 411-413 and 421-423 are developed on the photoresist 32. (column 3, lines 1-5)

Hsu et. al. develop the patterns in the last step of their method. It would have been obvious to one of ordinary skill in the art to implement the development step anywhere in the method disclosed by Hsu et. al. because ~~claim~~ ^{claim} 1 of the instant invention is written using open language, "comprising".

The step where the wafer is subjected to subsequent integrated forming steps could have been carried out anywhere in the method. For example,

the development step could have been carried out in between the two exposure steps as is done in the instant invention.

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-6 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Matsuoka et. al.

Matsuoka et. al. (Patent No. 5998068) disclose an invention where a reticle having a phase-shifting pattern and a normal pattern formed on a single reticle substrate is used to transfer by exposure the phase-shifting pattern and the normal pattern to each of the semiconductor chip regions of a resist film. A reticle according to this invention is for forming an island resist pattern. As shown in figure 2, the reticle 10A according to the first embodiment has a phase-shifting pattern region 11, a normal pattern (chromium pattern) region, and a shielding region 13 (column 5, lines 41-44). The mask disclosed by Matsuoka et. al. reads on the mask disclosed by the instant invention because it has two distinct patterns on it. First as shown in figure 4, the entire surface of a wafer 30 is coated with a resist material forming a resist film 31. Then, the phase-shifting pattern

region 11 and the normal pattern of the normal pattern region 12 are transferred in overlapping relation to each of the semiconductor chip regions of the resist film 31. (column 5, line 61 to column 6, line 16) In their invention Matsuoka et. al. claim that the semiconductor chip region exposed through the phase-shifting pattern region 11 is then exposed through the normal pattern region 12 in the subsequent shot (column 7, lines 30-34) The double exposure method claimed by Matsuoka et. al. reads on the double exposure method claimed by the instant invention.

Portions of the semiconductor chip region where the mask portions 11c of the phase-shifting pattern region 11 overlap the mask portions 12b of the normal pattern region 12 constitute a mask region (unexposed region). The resist film 31 is then prebaked and developed to provide a miniaturized island pattern formed in the mask region where the mask portion 11c of the phase-shifting pattern region 11 overlap the mask portions 12b of the normal pattern region 12. (column 7, lines 37-47) Thus, Matsuoka et. al. implement a processing step (prebaking and developing) after they expose the wafer twice.

Matsuoka et. al. develop the patterns in the last step of their method. It would have been obvious to one of ordinary skill in the art to implement the development step anywhere in the method disclosed by Matsuoka et. al. because claim 1 of the instant invention is written using open language, "comprising". The step where the wafer is subjected to subsequent

integrated forming steps could have been carried out anywhere in the method. For example, the development step could have been carried out in between the two exposure steps as is done in the instant invention.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shah Behshad whose telephone number is (571) 272-8948. The examiner can normally be reached on 8:30 - 17:00, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nam Nguyen can be reached on (571)272-1342. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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